

main surface of the base substrate 1 and the first electrode pads 1B on the back are eliminated, the electrode plates 8A and the electrode plate 8B can be arranged on the back of the base substrate 1. This allows the bump electrodes 4 to be freely located and shortens the distance between the bonding pads 2A of the semiconductor pellet 2 and the pump electrodes 4. As a result, the inductance can be reduced, thereby increasing the operating speeds of the semiconductor device.

The invention has been described in detail in connection with representative embodiments of the invention. It is noted, however, that the invention is not limited to these embodiments but that many modifications may be made without departing from the spirit of the invention.

Representative advantages of this invention may be summarized as follows.

It is possible to reduce the size of a semiconductor device in which the semiconductor pellet is mounted on the pellet mounting area of the main surface of the base substrate and in which the first electrode pads arranged on the back of the base substrate are electrically connected to the bonding pads arranged on the main surface of the semiconductor pellet.

It is possible to increase the operating speed of the semiconductor device.

It is also possible to enhance the electric reliability of the semiconductor device.

Further, it is possible to increase the mounting precision of the semiconductor device.

What is claimed is:

1. A semiconductor device comprising:

- (a) a rigid substrate having a first main surface and a second main surface opposite to the first main surface;
- (b) a semiconductor pellet mounted on the first main surface of the rigid substrate, the semiconductor pellet having a plurality of semiconductor circuit elements and a plurality of bonding pads;
- (c) a plurality of electrode pads formed on the second main surface of the rigid substrate; and
- (d) a plurality of bonding wires for electrically connecting the bonding pads of the semiconductor pellet with the electrode pads;

wherein the semiconductor pellet is mounted facedown on the rigid substrate, the rigid substrate has slits that extend from the first main surface to the second main surface and expose the bonding pads of the semiconductor pellet, the bonding wires extend through the slits in the rigid substrate to connect the bonding pads and the electrode pads, and bump electrodes are formed on said electrode pads.

2. A semiconductor device according to claim 1, wherein the bonding pads are arranged at the periphery of the semiconductor pellet and the slits are formed along the directions of rows of the bonding pads.

3. A semiconductor device according to claim 2, wherein the electrode pads are located on both sides of the slits.

4. A semiconductor device according to claim 3, wherein the electrode pads located on one side of the slits and under the semiconductor pellet are power supply pads, and the electrode pads located on the other side of the slits and outside the semiconductor pellet are signal pads.

5. A semiconductor device according to claim 1, further comprising a first resin sealing body covering the semiconductor pellet.

6. A semiconductor device according to claim 5, further comprising a second resin sealing body formed in the slits and covering the bonding wires.

8. A method of manufacturing a semiconductor device in which a semiconductor pellet is mounted on a pellet mounting area of the main surface of a rigid base substrate and in which first electrode pads arranged on the back of the rigid base substrate are electrically connected to bonding pads arranged on the main surface of the semiconductor pellet, said method comprising:

9. A method of manufacturing a semiconductor device according to claim 9, further comprising a step of forming by transfer molding a resin sealing body that covers the periphery of the main surface of the rigid base substrate and seals the bonding wires, after the step of electrically connecting the bonding wires.

11. A semiconductor device comprising:

- wherein the semiconductor pellet is mounted facedown on the rigid substrate, the rigid substrate has slits that extend from the first main surface to the second main surface and expose the bonding pads of the semiconductor pellet, and the bonding wires extend through the slits in the rigid substrate to connect the bonding pads and the electrode pads;

12. A semiconductor device according to claim 11, wherein the electrode pads are located on both sides of the slits.

14. A semiconductor device comprising:

- a substrate of a quadrilateral shape having a first pair of opposed edges and a second pair of opposed edges, said substrate having a first main surface, a second main surface opposite to said first main surface and a first slit

21. A semiconductor device according to claim 14, wherein said first electrode pads extend along said first and second slits, respectively, said second electrode pads extend along said first slit, and said third electrode pads extend along said second slit, wherein said first to third electrode

pads are arranged at a first pitch, respectively, wherein said bonding pads in said first and second slits are arranged at a second pitch which is smaller than said first pitch, respectively, wherein said bonding wires in said first slit alternately connect said bonding pads in said first slit with said first and second electrode pads, and wherein said bonding wires in said second slit alternately connect said bonding pads in said second slit with said first and third electrode pads.

22. A semiconductor device comprising:

- a substrate of a quadrilateral shape having first to fourth edges, said substrate having a first main surface, a second main surface opposite to said first main surface and first to fourth slits extending from said first main surface to said second main surface, said first to fourth slits respectively extending along said first to fourth edges and defining a first area of said substrate surrounded by said first to fourth slits and a second area of said substrate extending outside said first to fourth slits, said substrate having first electrode pads on said second main surface in said first area and second electrode pads on said second main surface in said second area;
- a semiconductor pellet having a main surface with semiconductor elements and bonding pads, said semiconductor pellet being mounted on said first main surface of substrate such that said bonding pads are arranged in line with said first to fourth slits;
- bonding wires extending through said first to fourth slits in said substrate and electrically connecting said bonding pads and said first and second electrode pads, respectively;
- a resin member sealing said semiconductor pellet and said bonding wires; and

bump electrodes arranged on said second main surface of said substrate in said first and second areas and being electrically connected with said first and second electrode pads.

wherein said bump electrodes in said second area are arranged to form a plurality of rows such that said plurality of rows are formed relative to one another to surround said first area of substrate.

23. A semiconductor device according to claim 22, wherein said semiconductor pellet has a quadrilateral shape and has first to fourth edges, wherein said bonding pads are arranged in a peripheral portion of said main surface and extend along said first to fourth edges of said semiconductor pellet.

24. A semiconductor device according to claim 23, wherein said semiconductor pellet is mounted on said first main surface opposite to said first area, wherein said substrate has a larger size than that of said semiconductor pellet, and wherein said bump electrodes in said second area are located outside said first to fourth edges of said semiconductor pellet.

25. A semiconductor device according to claim 22, wherein said first and second electrode pads extending along said first to fourth slits, respectively, and are arranged at a first pitch, wherein said bonding pads extend along said first and second electrode pads and are arranged at a second pitch which is smaller than said first pitch, and wherein said bonding wires alternately connect said bonding pads with said first and second electrode pads.

26. A semiconductor device comprising:

(1) a semiconductor pellet of a quadrilateral shape having bonding pads formed in a main surface thereof, said semiconductor pellet having a first pair of opposed edges extending in a first direction and a second pair of opposed edges extending in a second direction which intersects said first direction, said bonding pads being arranged in said first direction to form a row of bonding pads;

(2) a substrate having a first surface, a second surface opposite to said first surface, electrode pads formed on said second surface and a slit passing through said substrate from said first surface to said second surface and extending in said first direction, said semiconductor pellet being disposed on said first surface of said substrate such that said main surface of said semiconductor pellet is faced to said first surface of said substrate and said row of bonding pads are arranged in said slit in a plane view, said electrode pads including first electrode pads arranged at one side of said slit and second electrode pads arranged at the other side of said slit in said second direction;

(3) bonding wires electrically connecting said electrode pads of said substrate with said bonding pads of said semiconductor pellet via said slit, said bonding wires including first bonding wires connected to said first electrode pads and second bonding wires connected to said second electrode pads;

(5) a resin sealing body sealing said bonding wires and said main surface of said semiconductor pellet exposed from said slit.

28. A semiconductor device according to claim 26, wherein said semiconductor pellet has a rectangular shape, and wherein said first pair of opposed edges are corresponding to a pair of longer edges and said second pair of opposed edges are corresponding to a pair of shorter edges.

29. A semiconductor device according to claim 26, wherein
said slit is tapered so that opening on said second surface of

substrate is greater than opening on said first surface of said substrate.

30. A semiconductor device according to claim 26, wherein said bump electrodes are formed of a Pb-Sn alloy.

31. A semiconductor device according to claim 26, wherein said substrate is formed of a glass fiber impregnated with epoxy resin.

32. A semiconductor device according to claim 26, wherein said bonding wires are formed of gold.

33. A semiconductor device according to claim 32, wherein said bonding wires are connected to said bonding pads and said electrode pads by a bonding method that utilizes ultrasonic vibration in combination with thermo-compression.

34. A semiconductor device according to claim 26, wherein said substrate has land portions and conductors formed between said land portions and said electrode pads, wherein width of each of said land portions is larger than that of each of said conductors, wherein said land portions, said conductors and said electrode pads are integrally formed with one another on said second surface, and wherein said bump electrodes are arranged on said land portions.

35. A semiconductor device according to claim 34, wherein said substrate is formed of a single layer structure that has conductors arranged only on said second surface of said substrate.

36. A semiconductor device according to claim 26, wherein a pitch of said electrodes pads in said first direction is greater than a pitch of said bonding pads in said first direction.

37. A semiconductor device according to claim 26, wherein said substrate has a periphery which protrudes outwardly from said first and second pairs of opposed edges of said semiconductor pellet, wherein said first surface of said periphery of said substrate and said semiconductor pellet are sealed with a resin sealing body, and wherein a rear surface of said semiconductor pellet opposite to said main surface is exposed from said resin sealing body.

38. A semiconductor device according to claim 37, wherein said bump electrodes are arranged on said second surface of said substrate that overlap with said semiconductor pellet in said plane view and on said second surface of substrate at said periphery.

39. A semiconductor device comprising:

(1) a semiconductor pellet of a quadrilateral shape having bonding pads formed in a main surface thereof, said

semiconductor pellet having a first pair of opposed edges extending in a first direction and a second pair of opposed edges extending in a second direction which intersects said first direction, said bonding pads being arranged in said first direction to form a row of bonding pads;

(2) a substrate having a first surface, a second surface opposite to said first surface, electrode pads formed on said second surface and a slit passing through said substrate from said first surface to said second surface and extending in said first direction, said semiconductor pellet being disposed on said first surface of said substrate such that said main surface of said semiconductor pellet is faced to said first surface of said substrate and said row of bonding pads are arranged in said slit in a plane view, said electrode pads including first electrode pads arranged at one side of said slit and second electrode pads arranged at the other side of said slit in said second direction;

(3) bonding wires electrically connecting said electrode pads of said substrate with said bonding pads of said semiconductor pellet via said slit, said bonding wires including first bonding wires connected to said first electrode pads and second bonding wires connected to said second electrode pads;

(4) bump electrodes being disposed on said second surface of said substrate and being electrically connected to said electrode pads of said substrate, said bump electrodes including first bump electrodes electrically connected to said first electrode pads and arranged at said one side of said

slit and second bump electrodes electrically connected to said second electrode pads and arranged at the other side of said slit, said first bump electrodes being arranged in said first and second directions to form a matrix of bump electrodes, said second bump electrodes being arranged in said first and second directions to form a matrix of bump electrodes; and

(5) a resin sealing body sealing said bonding wires and said main surface of said semiconductor pellet exposed from said slit.

40. A semiconductor device according to claim 39, wherein said row of bonding pads is disposed at a substantially central area between said first pair of opposed edges of said semiconductor pellet.

41. A semiconductor device according to claim 39, wherein said semiconductor pellet has a rectangular shape, and wherein said first pair of opposed edges are corresponding to a pair of longer edges and said second pair of opposed edges are corresponding to a pair of shorter edges.

42. A semiconductor device according to claim 39, wherein said slit is tapered so that opening on said second surface of substrate is greater than opening on said first surface of said substrate.

43. A semiconductor device according to claim 39, wherein said bump electrodes are formed of a Pb-Sn alloy.

44. A semiconductor device according to claim 39, wherein said substrate is formed of a glass fiber impregnated with epoxy resin.

45. A semiconductor device according to claim 39, wherein said bonding wires are formed of gold.

46. A semiconductor device according to claim 45, wherein said bonding wires are connected to said bonding pads and said electrode pads by a bonding method that utilizes ultrasonic vibration in combination with thermo-compression.

47. A semiconductor device according to claim 39, wherein said substrate has land portions and conductors formed between said land portions and said electrode pads, wherein width of each of said land portions is larger than that of each of said conductors, wherein said land portions, said conductors and said electrode pads are integrally formed with one another on said second surface, and wherein said bump electrodes are arranged on said land portions.

48. A semiconductor device according to claim 47, wherein said substrate is formed of a single layer structure that has conductors arranged only on said second surface of said substrate.

49. A semiconductor device according to claim 39, wherein a pitch of said electrodes pads in said first direction is greater than a pitch of said bonding pads in said first direction.

50. A semiconductor device according to claim 39, wherein said substrate has a periphery which protrudes outwardly from said first and second pairs of opposed edges of said semiconductor pellet, wherein said first surface of said periphery of said substrate and said semiconductor pellet are sealed with a resin sealing body, and wherein a rear surface of said semiconductor pellet opposite to said main surface is exposed from said resin sealing body.

51. A semiconductor device according to claim 50, wherein said bump electrodes are arranged on said second surface of said substrate that overlap with said semiconductor pellet in said plane view and on said second surface of substrate at said periphery.

52. A semiconductor device comprising:

(1) a semiconductor pellet of a quadrilateral shape having bonding pads formed in a main surface thereof, said semiconductor pellet having a first pair of opposed edges extending in a first direction and a second pair of opposed edges extending in a second direction which intersects said first direction, said bonding pads being arranged in said first direction to form a row of bonding pads;

(2) a substrate having a first surface, a second surface opposite to said first surface, electrode pads formed on said second surface and a slit passing through said substrate from said first surface to said second surface and extending in said first direction, said semiconductor pellet being disposed on said first surface of said substrate such that said main surface of said semiconductor pellet is faced to said first surface of said substrate and said row of bonding pads are arranged in said slit in a plane view, said electrode pads including first electrode pads arranged at one side of said slit and second electrode pads arranged at the other side of said slit in said second direction;

(3) an insulating layer of a low-elasticity resin formed between said substrate and said semiconductor chip to expose said row of bonding pads;

(4) conductors electrically connecting said electrode pads of said substrate with said bonding pads of said semiconductor pellet via said slit, said conductors including first conductors connected to said first electrode pads and second conductors connected to said second electrode pads;

(5) bump electrodes being disposed on said second surface of said substrate and being electrically connected to said electrode pads of said substrate, said bump electrodes including first bump electrodes electrically connected to said first electrode pads and arranged at said one side of said slit and second bump electrodes electrically connected to said second electrode pads and arranged at the other side of said slit, said first and second bump electrodes being arranged to

overlap with said semiconductor pellet in said plane view respectively; and

(6) a resin sealing body sealing said conductors and said main surface of said semiconductor pellet exposed from said slit.

53. A semiconductor device according to claim 52, wherein said row of bonding pads is disposed at a substantially central area between said first pair of opposed edges of said semiconductor pellet.

54. A semiconductor device according to claim 52, wherein said semiconductor pellet has a rectangular shape, and wherein said first pair of opposed edges are corresponding to a pair of longer edges and said second pair of opposed edges are corresponding to a pair of shorter edges.

55. A semiconductor device according to claim 52, wherein said slit is tapered so that opening on said second surface of substrate is greater than opening on said first surface of said substrate.

56. A semiconductor device according to claim 52, wherein said bump electrodes are formed of a Pb-Sn alloy.

57. A semiconductor device according to claim 52, wherein said substrate is formed of a glass fiber impregnated with epoxy resin.

58. A semiconductor device according to claim 52, wherein said bonding wires are formed of gold.

59. A semiconductor device according to claim 58, wherein said bonding wires are connected to said bonding pads and said electrode pads by a bonding method that utilizes ultrasonic vibration in combination with thermo-compression.

60. A semiconductor device according to claim 52, wherein said substrate has land portions and conductors formed between said land portions and said electrode pads, wherein width of each of said land portions is larger than that of each of said conductors, wherein said land portions, said conductors and said electrode pads are integrally formed with one another on said second surface, and wherein said bump electrodes are arranged on said land portions.

61. A semiconductor device according to claim 60, wherein said substrate is formed of a single layer structure that has conductors arranged only on said second surface of said substrate.

62. A semiconductor device according to claim 52, wherein a pitch of said electrodes pads in said first direction is greater than a pitch of said bonding pads in said first direction.

63. A semiconductor device according to claim 52, wherein said substrate has a periphery which protrudes outwardly from said first and second pairs of opposed edges of said semiconductor pellet, wherein said first surface of said periphery of said substrate and said semiconductor pellet are sealed with a resin sealing body, and wherein a rear surface of said semiconductor pellet opposite to said main surface is exposed from said resin sealing body.

64. A semiconductor device according to claim 63, wherein .said bump electrodes are arranged on said second surface of said substrate that overlap with said semiconductor pellet in said plane view and on said second surface of substrate at said periphery.

65. A semiconductor device according to claim 52, wherein said insulating layer is a selected one of either polyimide-, epoxy-, or silicon-base low-elasticity resin.

66. A semiconductor device comprising:

(1) a semiconductor pellet of a quadrilateral shape having bonding pads formed in a main surface thereof, said semiconductor pellet having a first pair of opposed edges extending in a first direction and a second pair of opposed edges extending in a second direction which intersects said first direction, said bonding pads being arranged in said first direction to form a row of bonding pads;

(3) an insulating layer of a low-elasticity resin formed between said substrate and said semiconductor chip to expose said row of bonding pads;

(5) bump electrodes being disposed on said second surface of said substrate and being electrically connected to said electrode pads of said substrate, said bump electrodes including first bump electrodes electrically connected to said first electrode pads and arranged at said one side of said slit and second bump electrodes electrically connected to said second electrode pads and arranged at the other side of said slit, said first bump electrodes being arranged in said first

and second directions to form a matrix of bump electrodes, said second bump electrodes being arranged in said first and second directions to form a matrix of bump electrodes; and

(6) a resin sealing body sealing said conductors and said main surface of said semiconductor pellet exposed from said slit.

67. A semiconductor device according to claim 66, wherein said row of bonding pads is disposed at a substantially central area between said first pair of opposed edges of said semiconductor pellet.

68. A semiconductor device according to claim 66, wherein said semiconductor pellet has a rectangular shape, and wherein said first pair of opposed edges are corresponding to a pair of longer edges and said second pair of opposed edges are corresponding to a pair of shorter edges.

69. A semiconductor device according to claim 66, wherein said slit is tapered so that opening on said second surface of substrate is greater than opening on said first surface of said substrate.

70. A semiconductor device according to claim 66, wherein said bump electrodes are formed of a Pb-Sn alloy.

71. A semiconductor device according to claim 66, wherein said substrate is formed of a glass fiber impregnated with epoxy resin.

72. A semiconductor device according to claim 66, wherein said bonding wires are formed of gold.

73. A semiconductor device according to claim 72, wherein said bonding wires are connected to said bonding pads and said electrode pads by a bonding method that utilizes ultrasonic vibration in combination with thermo-compression.

74. A semiconductor device according to claim 66, wherein said substrate has land portions and conductors formed between said land portions and said electrode pads, wherein width of each of said land portions is larger than that of each of said conductors, wherein said land portions, said conductors and said electrode pads are integrally formed with one another on said second surface, and wherein said bump electrodes are arranged on said land portions.

75. A semiconductor device according to claim 74, wherein said substrate is formed of a single layer structure that has conductors arranged only on said second surface of said substrate.

76. A semiconductor device according to claim 66, wherein a pitch of said electrodes pads in said first direction is greater than a pitch of said bonding pads in said first direction.

77. A semiconductor device according to claim 66, wherein said substrate has a periphery which protrudes outwardly from said first and second pairs of opposed edges of said semiconductor pellet, wherein said first surface of said periphery of said substrate and said semiconductor pellet are sealed with a resin sealing body, and wherein a rear surface of said semiconductor pellet opposite to said main surface is exposed from said resin sealing body.

78. A semiconductor device according to claim 77, wherein said bump electrodes are arranged on said second surface of said substrate that overlap with said semiconductor pellet in said plane view and on said second surface of substrate at said periphery.

79. A semiconductor device according to claim 66, wherein said insulating layer is a selected one of either polyimide-, epoxy-, or silicon-base low-elasticity resin.

80. A semiconductor device comprising:

(1) a semiconductor pellet having bonding pads formed in a main surface thereof, said bonding pads including first

bonding pads for signals and second bonding pads for a power source;

(2) a substrate having a first surface, a second surface opposite to said first surface, electrode pads formed on said second surface and a slit passing through said substrate from said first surface to said second surface, said electrode pads including first electrode pads for signals and a second electrode pad for a power source, said semiconductor pellet being disposed on said first surface of said substrate such that said main surface of said semiconductor pellet is faced to said first surface of said substrate and said bonding pads are arranged in said slit in a plane view;

(3) an insulating layer of a low-elasticity resin formed between said substrate and said semiconductor chip to expose said bonding pads;

(4) conductors electrically connecting said electrode pads with said bonding pads of said semiconductor pellet via said slit, said conductors including first conductors connecting said first bonding pads with said first electrode pads for said signals respectively and second conductors connecting said second bonding pads with said second electrode pad for said power source;

(5) bump electrodes being disposed on said second surface of said substrate and being electrically connected to said electrode pads of said substrate, said bump electrodes including first bump electrodes electrically connected to said first electrode pads for said signals respectively and second

bump electrodes electrically connected to said second electrode pad for said power source; and

(6) a resin sealing body sealing said conductors and said main surface of said semiconductor pellet exposed from said slit, wherein an area of said second electrode pad for said power source is larger than that of each of said first electrode pads, and wherein said second bump electrodes are disposed on said second electrode pad for said power source and are in electrical common connection to said second electrode pad.

81. A semiconductor device according to claim 80, wherein said power source is either a reference voltage or an operating voltage.

82. A semiconductor device according to claim 80, wherein said insulating layer is a selected one of either polyimide-, epoxy-, or silicon-base low-elasticity resin.

83. A semiconductor device according to claim 80, wherein said bump electrodes are formed of a Pb-Sn alloy.

84. A semiconductor device according to claim 80, wherein said substrate is formed of a glass fiber impregnated with epoxy resin.

002020-THSE-950

86. A semiconductor device according to claim 26, wherein
said semiconductor pellet includes a circuit system formed in
said main surface thereof.

88. A semiconductor device according to claim 52, wherein
said semiconductor pellet includes a circuit system formed in
said main surface thereof.

89. A semiconductor device according to claim 66, wherein
said semiconductor pellet includes a circuit system formed in
said main surface thereof.

90. A semiconductor device according to claim 80, wherein
said semiconductor pellet includes a circuit system formed in
said main surface thereof.